

# Low-Voltage CMOS Hex Buffer with Open Drain Outputs

With 5 V-Tolerant Inputs

## MC74LCX07

The MC74LCX07 is a high performance hex buffer operating from a 1.65 to 5.5 V supply. High impedance TTL compatible inputs significantly reduce current loading to input drivers. These LCX devices have open drain outputs which provide the ability to set output levels, or do active-HIGH AND or active-LOW OR functions. A  $V_I$  specification of 5.5 V allows MC74LCX07 inputs to be safely driven from 5.0 V devices.

### Features

- Designed for 1.65 to 5.5 V  $V_{CC}$  Operation
- 5.0 V Tolerant Inputs/Outputs
- LVTTTL Compatible
- LVC MOS Compatible
- 24 mA Output Sink Capability @ 3.0 V
- Near Zero Static Supply Current (10  $\mu$ A) Substantially Reduces System Power Requirements
- Latchup Performance Exceeds 100 mA
- Wired-OR, Wired-AND
- Output Level Can Be Set Externally Without Affecting Speed of Device
- ESD Performance: Human Body Model >2000 V
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

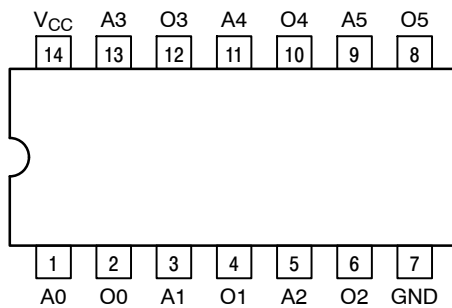
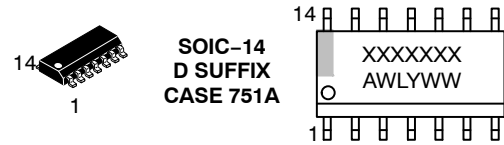


Figure 1. Pinout: 14-Lead (Top View)

### MARKING DIAGRAMS



XXXXXX = Specific Device Code  
 A = Assembly Location  
 L, WL = Wafer Lot  
 Y, YY = Year  
 W, WW = Work Week  
 G or ■ = Pb-Free Package  
 (Note: Microdot may be in either location)

### ORDERING INFORMATION

See detailed ordering and shipping information on page 5 of this data sheet.

# MC74LCX07

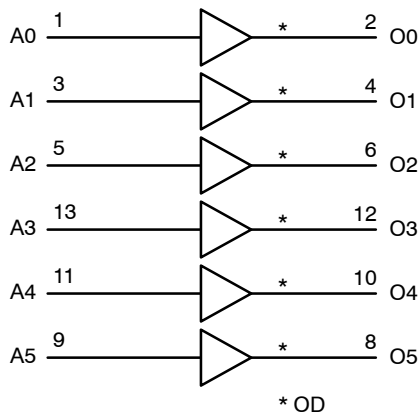


Figure 2. Logic Diagram

## PIN NAMES

Pins	Function
An On	Data Inputs Outputs

## TRUTH TABLE

An	On
L	L
H	Z

## MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
$V_{CC}$	DC Supply Voltage	-0.5 to +6.5	V
$V_I$	DC Input Voltage (Note 1)	-0.5 to +6.5	V
$V_O$	DC Output Voltage (Note 1)	Active-Mode (High or Low State) Tri-State Mode Power-Down Mode ( $V_{CC} = 0$ V)	-0.5 to $V_{CC} + 0.5$ -0.5 to +6.5 -0.5 to +6.5
$I_{IK}$	DC Input Diode Current	$V_I < GND$	-50 mA
$I_{OK}$	DC Output Diode Current	$V_O < GND$	-50 mA
$I_O$	DC Output Source/Sink Current		$\pm 50$ mA
$I_{CC}$ or $I_{GND}$	DC Supply Current per Supply Pin or Ground Pin		$\pm 100$ mA
$T_{STG}$	Storage Temperature Range		-65 to +150 °C
$T_L$	Lead Temperature, 1 mm from Case for 10 secs		260 °C
$T_J$	Junction Temperature Under Bias		+150 °C
$\theta_{JA}$	Thermal Resistance (Note 1)	SOIC-14 QFN14 TSSOP-14	116 130 150 °C/W
$P_D$	Power Dissipation in Still Air at 125°C	SOIC-14 QFN14 TSSOP-14	1077 962 833 mW
MSL	Moisture Sensitivity		Level 1 -
$F_R$	Flammability Rating	Oxygen Index: 28 to 34	UL 94 V-0 @ 0.125 in -
$V_{ESD}$	ESD Withstand Voltage (Note 3)	Human Body Model Charged Device Model	2000 N/A V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

- $I_O$  absolute maximum rating must be observed.
- Measured with minimum pad spacing on an FR4 board, using 76mm-by-114mm, 2-ounce copper trace no air flow per JESD51-7.
- HBM tested to EIA / JESD22-A114-A. CDM tested to JESD22-C101-A. JEDEC recommends that ESD qualification to EIA/JESD22-A115A (Machine Model) be discontinued.

# MC74LCX07

## RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Typ	Max	Unit	
V <sub>CC</sub>	Supply Voltage	Operating	1.65	3.3	5.5	V
		Data Retention Only	1.5	3.3	5.5	
V <sub>I</sub>	Digital Input Voltage	0	–	5.5	V	
V <sub>O</sub>	Output Voltage	Active Mode (High or Low State)	0	–	V <sub>CC</sub>	V
		Tri-State Mode	0	–	5.5	
		Power Down Mode (V <sub>CC</sub> = 0 V)	0	–	5.5	
T <sub>A</sub>	Operating Free-Air Temperature	–40	–	+125	°C	
t <sub>r</sub> , t <sub>f</sub>	Input Rise or Fall Rate	V <sub>CC</sub> = 1.65 V to 1.95 V	0	–	20	nS/V
		V <sub>CC</sub> = 2.3 V to 2.7 V	0	–	20	
		V <sub>I</sub> from 0.8 V to 2.0 V, V <sub>CC</sub> = 3.0 V	0	–	10	
		V <sub>CC</sub> = 4.5 V to 5.5 V	0	–	5	

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

4. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V<sub>CC</sub>). Unused outputs must be left open.

## DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Conditions	V <sub>CC</sub> (V)	T <sub>A</sub> = –40°C to +85°C		T <sub>A</sub> = –40°C to +125°C		Unit
				Min	Max	Min	Max	
V <sub>IH</sub>	HIGH Level Input Voltage		1.65 – 1.95	0.65 x V <sub>CC</sub>	–	0.65 x V <sub>CC</sub>	–	V
			2.3 – 2.7	1.7	–	1.7	–	
			3.0 – 3.6	2.0	–	2.0	–	
			4.5 – 5.5	0.70 x V <sub>CC</sub>	–	0.70 x V <sub>CC</sub>	–	
V <sub>IL</sub>	LOW Level Input Voltage		1.65 – 1.95	–	0.35 x V <sub>CC</sub>	–	0.35 x V <sub>CC</sub>	V
			2.3 – 2.7	–	0.7	–	0.7	
			3.0 – 3.6	–	0.8	–	0.8	
			4.5 – 5.5	–	0.30 x V <sub>CC</sub>	–	0.30 x V <sub>CC</sub>	
V <sub>OL</sub>	Low-Level Output Voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> I <sub>OL</sub> = 100 μA I <sub>OL</sub> = 4 mA I <sub>OL</sub> = 8 mA I <sub>OL</sub> = 12 mA I <sub>OL</sub> = 16 mA I <sub>OL</sub> = 24 mA I <sub>OL</sub> = 32 mA	1.65 to 5.5	–	0.1	–	0.1	V
			1.65	–	0.24	–	0.24	
			2.3	–	0.3	–	0.3	
			2.7	–	0.4	–	0.4	
			3.0	–	0.4	–	0.4	
			3.0	–	0.55	–	0.55	
			4.5	–	0.6	–	0.6	
I <sub>I</sub>	Input Leakage Current	V <sub>I</sub> = 0 to 5.5 V	3.6	–	±5.0	–	±5.0	μA
I <sub>OFF</sub>	Power Off Leakage Current	V <sub>I</sub> = 5.5 V or V <sub>O</sub> = 5.5 V	0	–	10	–	10	μA
I <sub>CC</sub>	Quiescent Supply Current	V <sub>I</sub> = 5.5 V or GND	3.6	–	10	–	10	μA
ΔI <sub>CC</sub>	Increase in I <sub>CC</sub> per Input	One input at V <sub>CC</sub> – 0.6 V, other inputs at V <sub>CC</sub> or GND	2.3 to 3.6	–	500	–	500	μA
			4.5 to 5.5	–	1.0	–	1.0	mA
		One input at 3.125 V, other inputs at V <sub>CC</sub> or GND	5.25	–	10	–	10	

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

# MC74LCX07

## AC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Condition	V <sub>CC</sub> (V)	T <sub>A</sub> = -40°C to +85°C		T <sub>A</sub> = -40°C to +125°C		Unit
				Min	Max	Min	Max	
t <sub>pLZ</sub> , t <sub>pZL</sub>	Propagation Delay, Input to Output	See Figures 3 and 4	1.65 to 1.95	-	6.5	-	6.5	ns
			2.3 to 2.7	-	3.8	-	3.8	
			2.7	-	3.7	-	3.7	
			3.0 to 3.6	-	3.0	-	3.3	
			4.5 to 5.5	-	2.7	-	2.7	

## DYNAMIC SWITCHING CHARACTERISTICS

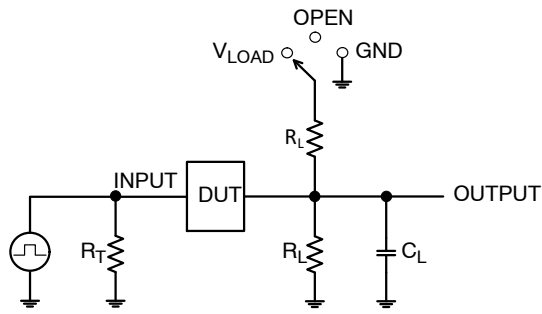
Symbol	Characteristic	Condition	T <sub>A</sub> = +25°C			Unit
			Min	Typ	Max	
V <sub>OLP</sub>	Dynamic LOW Peak Voltage (Note 5)	V <sub>CC</sub> = 3.3 V, C <sub>L</sub> = 50 pF, V <sub>IH</sub> = 3.3 V, V <sub>IL</sub> = 0 V V <sub>CC</sub> = 2.5 V, C <sub>L</sub> = 30 pF, V <sub>IH</sub> = 2.5 V, V <sub>IL</sub> = 0 V		0.9 0.7		V
V <sub>OLV</sub>	Dynamic LOW Valley Voltage (Note 5)	V <sub>CC</sub> = 3.3 V, C <sub>L</sub> = 50 pF, V <sub>IH</sub> = 3.3 V, V <sub>IL</sub> = 0 V V <sub>CC</sub> = 2.5 V, C <sub>L</sub> = 30 pF, V <sub>IH</sub> = 2.5 V, V <sub>IL</sub> = 0 V		-0.8 -0.6		V

5. Number of outputs defined as "n". Measured with "n-1" outputs switching from HIGH-to-LOW or LOW-to-HIGH. The remaining output is measured in the LOW state.

## CAPACITIVE CHARACTERISTICS

Symbol	Parameter	Condition	Typ	Unit
C <sub>IN</sub>	Input Capacitance	V <sub>CC</sub> = 3.3 V, V <sub>I</sub> = 0 V or V <sub>CC</sub>	7	pF
C <sub>OUT</sub>	Output Capacitance	V <sub>CC</sub> = 3.3 V, V <sub>I</sub> = 0 V or V <sub>CC</sub>	8	pF
C <sub>PD</sub>	Power Dissipation Capacitance	10 MHz, V <sub>CC</sub> = 3.3 V, V <sub>I</sub> = 0 V or V <sub>CC</sub>	25	pF

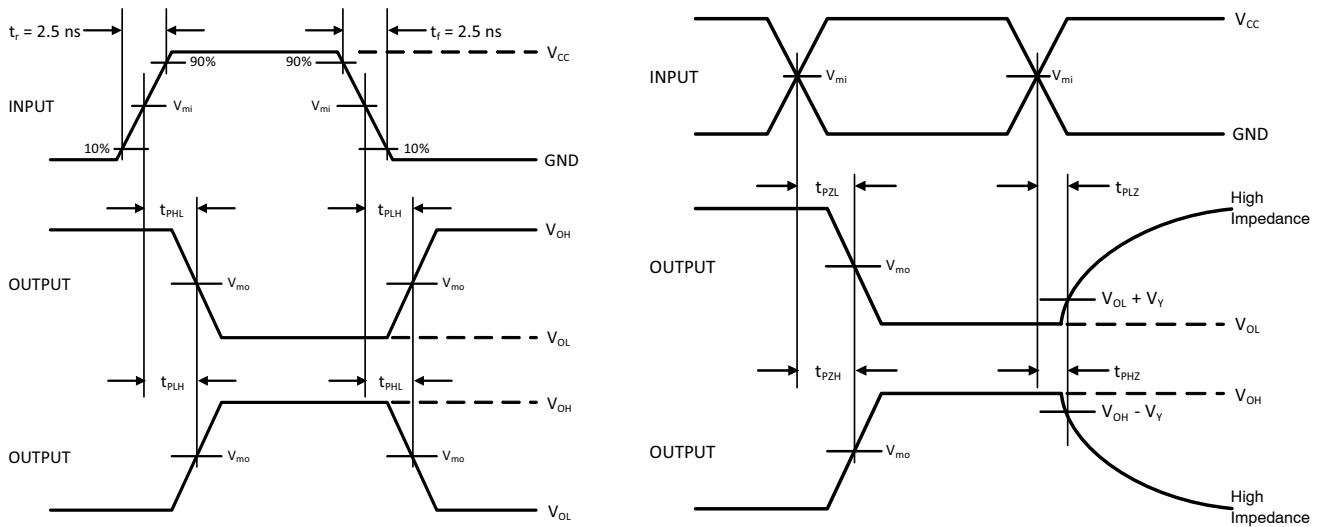
# MC74LCX07



$C_L$  includes probe and jig capacitance  
 $R_T$  is  $Z_{OUT}$  of pulse generator (typically 50  $\Omega$ )  
 $f = 1$  MHz

Test	Switch Position
$t_{PLH} / t_{PHL}$	Open
$t_{PLZ} / t_{PZL}$	$V_{LOAD}$
$t_{PHZ} / t_{PZH}$	GND

Figure 3. Test Circuit



$V_{CC}, V$	$R_L, \Omega$	$C_L, pF$	$V_{LOAD}$	$V_m, V$	$V_Y, V$
1.65 to 1.95	500	30	$2 \times V_{CC}$	$V_{CC}/2$	0.15
2.3 to 2.7	500	30	$2 \times V_{CC}$	$V_{CC}/2$	0.15
2.7	500	50	6 V	1.5	0.3
3.0 to 3.6	500	50	6 V	1.5	0.3
4.5 to 5.5	500	50	$2 \times V_{CC}$	$V_{CC}/2$	0.3

Figure 4. Switching Waveforms

## ORDERING INFORMATION

Device	Marking	Package	Shipping <sup>†</sup>
MC74LCX07DG	LCX07G	SOIC-14	55 Units / Rail
MC74LCX07DR2G	LCX07G	SOIC-14	2500 / Tape & Reel
MC74LCX07DTR2G	LCX 07	TSSOP-14	2500 / Tape & Reel

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

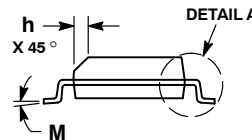
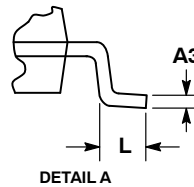
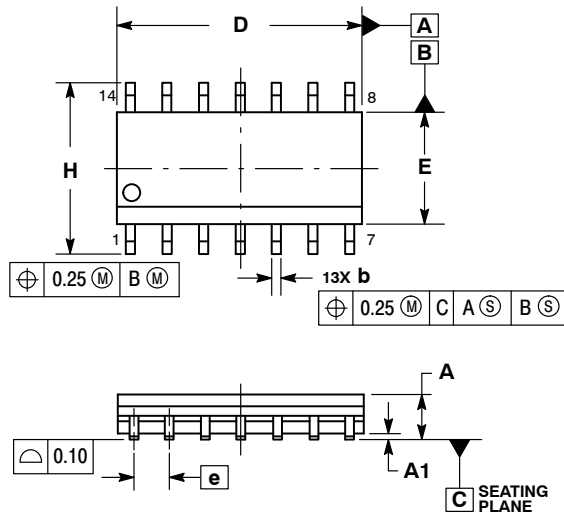
\*-Q Suffix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable.



SCALE 1:1

SOIC-14 NB  
CASE 751A-03  
ISSUE L

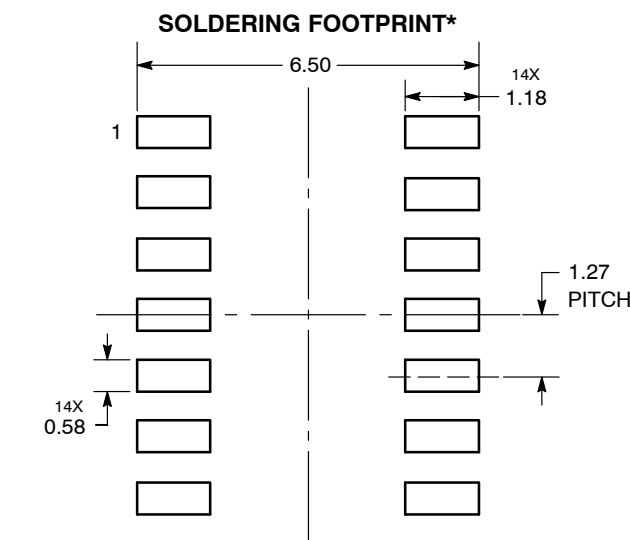
DATE 03 FEB 2016



NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF AT MAXIMUM MATERIAL CONDITION.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSIONS.
5. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.

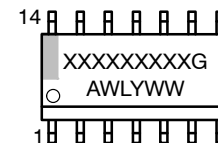
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	1.35	1.75	0.054	0.068
A1	0.10	0.25	0.004	0.010
A3	0.19	0.25	0.008	0.010
b	0.35	0.49	0.014	0.019
D	8.55	8.75	0.337	0.344
E	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
H	5.80	6.20	0.228	0.244
h	0.25	0.50	0.010	0.019
L	0.40	1.25	0.016	0.049
M	0°	7°	0°	7°



DIMENSIONS: MILLIMETERS

\*For additional information on our Pb-Free strategy and soldering details, please download the onsemi Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM\*



- XXXXXX = Specific Device Code
- A = Assembly Location
- WL = Wafer Lot
- Y = Year
- WW = Work Week
- G = Pb-Free Package

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

STYLES ON PAGE 2

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**SOIC-14**  
**CASE 751A-03**  
**ISSUE L**

DATE 03 FEB 2016

STYLE 1:  
 PIN 1. COMMON CATHODE  
 2. ANODE/CATHODE  
 3. ANODE/CATHODE  
 4. NO CONNECTION  
 5. ANODE/CATHODE  
 6. NO CONNECTION  
 7. ANODE/CATHODE  
 8. ANODE/CATHODE  
 9. ANODE/CATHODE  
 10. NO CONNECTION  
 11. ANODE/CATHODE  
 12. ANODE/CATHODE  
 13. NO CONNECTION  
 14. COMMON ANODE

STYLE 2:  
 CANCELLED

STYLE 3:  
 PIN 1. NO CONNECTION  
 2. ANODE  
 3. ANODE  
 4. NO CONNECTION  
 5. ANODE  
 6. NO CONNECTION  
 7. ANODE  
 8. ANODE  
 9. ANODE  
 10. NO CONNECTION  
 11. ANODE  
 12. ANODE  
 13. NO CONNECTION  
 14. COMMON CATHODE

STYLE 4:  
 PIN 1. NO CONNECTION  
 2. CATHODE  
 3. CATHODE  
 4. NO CONNECTION  
 5. CATHODE  
 6. NO CONNECTION  
 7. CATHODE  
 8. CATHODE  
 9. CATHODE  
 10. NO CONNECTION  
 11. CATHODE  
 12. CATHODE  
 13. NO CONNECTION  
 14. COMMON ANODE

STYLE 5:  
 PIN 1. COMMON CATHODE  
 2. ANODE/CATHODE  
 3. ANODE/CATHODE  
 4. ANODE/CATHODE  
 5. ANODE/CATHODE  
 6. NO CONNECTION  
 7. COMMON ANODE  
 8. COMMON CATHODE  
 9. ANODE/CATHODE  
 10. ANODE/CATHODE  
 11. ANODE/CATHODE  
 12. ANODE/CATHODE  
 13. NO CONNECTION  
 14. COMMON ANODE

STYLE 6:  
 PIN 1. CATHODE  
 2. CATHODE  
 3. CATHODE  
 4. CATHODE  
 5. CATHODE  
 6. CATHODE  
 7. CATHODE  
 8. ANODE  
 9. ANODE  
 10. ANODE  
 11. ANODE  
 12. ANODE  
 13. ANODE  
 14. ANODE

STYLE 7:  
 PIN 1. ANODE/CATHODE  
 2. COMMON ANODE  
 3. COMMON CATHODE  
 4. ANODE/CATHODE  
 5. ANODE/CATHODE  
 6. ANODE/CATHODE  
 7. ANODE/CATHODE  
 8. ANODE/CATHODE  
 9. ANODE/CATHODE  
 10. ANODE/CATHODE  
 11. COMMON CATHODE  
 12. COMMON ANODE  
 13. ANODE/CATHODE  
 14. ANODE/CATHODE

STYLE 8:  
 PIN 1. COMMON CATHODE  
 2. ANODE/CATHODE  
 3. ANODE/CATHODE  
 4. NO CONNECTION  
 5. ANODE/CATHODE  
 6. ANODE/CATHODE  
 7. COMMON ANODE  
 8. COMMON ANODE  
 9. ANODE/CATHODE  
 10. ANODE/CATHODE  
 11. NO CONNECTION  
 12. ANODE/CATHODE  
 13. ANODE/CATHODE  
 14. COMMON CATHODE

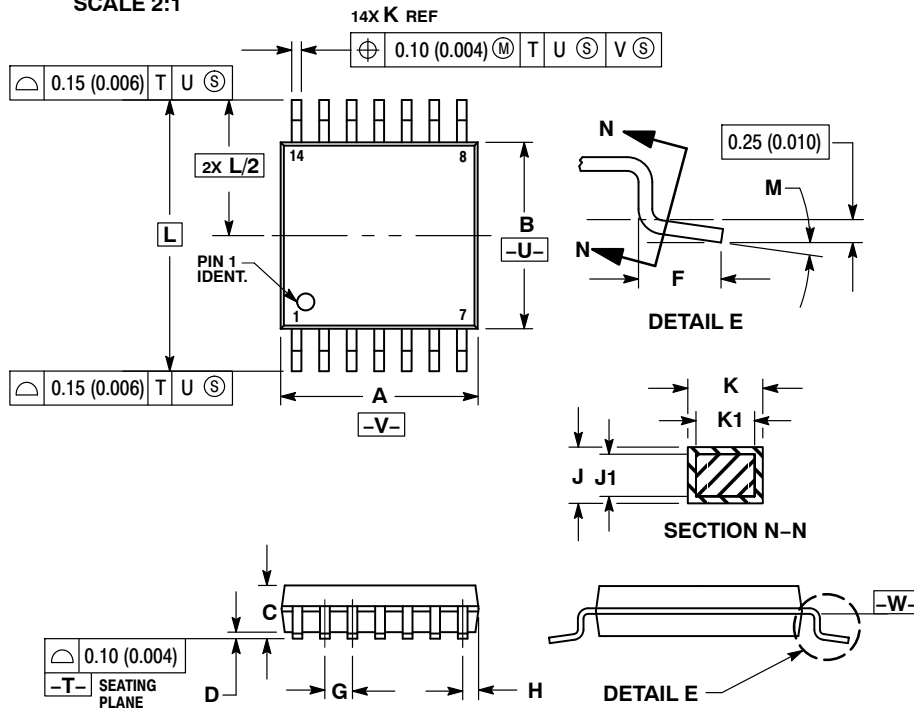
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TSSOP-14 WB  
CASE 948G  
ISSUE C

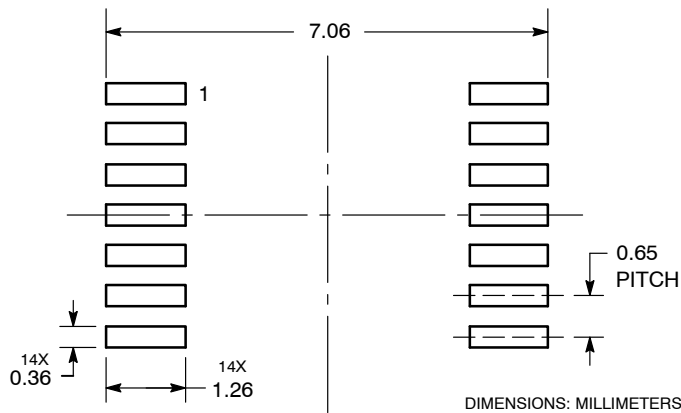
DATE 17 FEB 2016



- NOTES:
- DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  - CONTROLLING DIMENSION: MILLIMETER.
  - DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
  - DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
  - DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
  - TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
  - DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

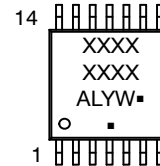
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	---	1.20	---	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.50	0.60	0.020	0.024
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

RECOMMENDED  
SOLDERING FOOTPRINT\*



\*For additional information on our Pb-Free strategy and soldering details, please download the onsemi Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC  
MARKING DIAGRAM\*



- A = Assembly Location
- L = Wafer Lot
- Y = Year
- W = Work Week
- = Pb-Free Package

(Note: Microdot may be in either location)

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

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